REMARKS

No new matter is added by this amendment. The present application was filed on February 24, 2002, with original claims 1-37, 36(2), 37(2) and 38-58. The claims have been renumbered as claims 1-60. Claims 36(2) and 37(2) have been renumbered as claims and 38 and 39, respectively, and original claims 38-58 have been renumbered as claims 40-60. The renumbering of the claims are shown as amendments above. By this present amendment, claims, 35-37 and renumbered claims 38, 44, 46, 48-52, and 54-58 have been amended, and renumbered claims 59 and 60 have been cancelled without prejudice to reduce the number of issues remaining in the application. The claims remaining in consideration are claims 1-58. Claims 1, 11, 20, 34, 47, and 53 are independent. Reconsideration is respectfully requested.

Claims 35-38, 48-49, and 54-58 were rejected under 35 USC §112. Claims 35-38, 48-49, 51, and 54-58 have been amended to correct the deficiencies noted by the Examiner. Applicants therefore request that the §112 rejection be withdrawn.

The Examiner noted that claims 6-8, 15, 29-31, and 42 (original claim 40), contained allowable subject matter. This is noted with appreciated.

Claims 1-5, 9-14, 18-22, 24-28, 32, 33, 34, 39, 40, 41, 45-47, 52-53 and 58 were rejected under 35 USC §103(a) as being unpatentable over Fennel et al ("Fennel") and Heugel et al ("Heugel"). This rejection is respectively traversed.

The present invention as set forth in independent claim 1, sets forth a controller with primary and secondary processing units **12, 14**, a common memory **16** and a functional compare module **18**. The secondary processing unit **14** is coupled to the primary processing unit **14**. The common memory **16** is coupled to the primary and secondary processing units **12, 14**. The common memory **16** contains a control algorithm. The primary and secondary processing units **12, 14** are adapted to run the control algorithm. The functional compare module **18** is coupled to the primary processing unit **12** and the secondary processing unit **14** and compares a primary output of the primary processing unit and a secondary output of the secondary processing units after the control algorithm has been run by the primary and secondary processing units.

Figure 2 of Fennel discloses a control system with two microprocessors 250, 251. Each microprocessor 250, 251 has its own main function (see column 1, lines 48-53), but can exchange data (column 1, lines 63-64). Each microprocessor receives the same sensor signals (through the other microprocessor, and "the controlling or regulating task may be processed in parallel in the other microprocessor" (Column 4, lines 29-31).

However, contrary to the Examiner's assertions, Fennel does not disclose a separate function control module **18**, rather the "result can be transmitted by way of the data bus ***and compared in one of the microprocessors***" (column 4, lines 31-33, emphasis added). Thus, Fennel teaches award from the claimed invention in that it requires that one of the microprocessors dedicate computing cycles to this task.

The Examiner recognizes that Fennel does not teach the common memory of independent claim 1, but utilizes Heugel to teach a common memory. It should be noted that Heugel discloses a multi-processor system with two processors, **each** having their own local memory (see Abtract). The Heugel system allows each processor to read and write to the local memory of the other processor.

Since neither Heugel nor Fennel teach or disclose at least one element of independent claim 1, applicants respectfully assert that the §103(a) rejection is improper and request that it be withdrawn.

Claims 2-5 and 9-10 are ultimately dependent upon allowable claim 1. Therefore, for the reasons set forth above, and based on their own merits, applicants respectfully assert that claims 2-5 and 9-10 are also allowable.

Independent claim 11 sets forth a method for detecting a fault in a controller. The controller includes a primary processing unit, a secondary processing unit coupled to the primary processing unit, and a common memory coupled to the secondary and primary processing units. The method includes the steps of reading a control algorithm stored in the common memory by the primary processing unit, reading the control algorithm stored in the common memory by the secondary processing unit, and comparing a primary output of the primary processing unit and a secondary output of the secondary processing unit and responsively detecting a fault.

The Examiner refers to column 2, lines 7-10, stating "Fennel also teaches reading a control algorithm stored in the common memory by the primary processing unit" and "Fennel also teaches reading the control algorithm stored in the common memory by the second processing unit" (See page 6, last and second from the last paragraphs). However, the lines referred to by the Examiner make no such teaching, i.e., it states that "... the data necessary for perfuming at least part of the controlling or regulating task of the first control unit are also supplied to at least one further control unit". As stated above, this apparently is done by transferring data from the sensor(s) from one control unit to the other.

Furthermore, the Examiner correctly stated in the rejection to claim 1, that Fennel does not include the common memory.

Thus, Fennel cannot include the steps of reading the control algorithm from the common memory by both processing units.

Heugel also does not teach the steps of reading the control algorithm from the common memory by both processing units. As stated above, Heugel discloses a multi-processor system with two processors, **each** having their own local memory (see Abtract). The Heugel system does allow each processor to read and write to the local memory of the other processor. However, Heugel does not teach the steps of reading the same control algorithm from a common memory by two processors. In fact, in the disclosed embodiment, the processors in the Heugel system ***cannot*** read from the portion of the memory that contains program code:

> Software running on the MPU's 24, 24' uses a memory model that divides the local RAM 20, 20' of each MPU 24, 24' into ***program area (which is not shared or mirrored with the paired MPU),*** a system memory area (a pool of allocatable local RAM that is pride to the local MPU), and allocatable mirrored memory area which is maintained as an "equalized" data area.... .
>
> (Column 6, lines 5-9, emphasis added).

Since neither Fennel nor Heugel disclose all of the elements of independent claim 11, applicants respectfully assert that the §103(a) rejection of independent claim 11 and request that it be withdrawn.

Claims 12-14, 18, and 19 are ultimately dependent upon allowable claim 1. Therefore, for the reasons set forth above and based on their own merits, applicants respectfully assert that claims 12-14, 18 and 19 are also allowable.

Independent claim 20 sets forth an apparatus for controlling a first system of a motor vehicle. The apparatus includes primary and secondary processing units, a common memory, and a functional compare module. The primary processing unit performs a first set of functions with respect to the first system. The secondary processing unit is coupled to the primary processing unit. The common memory is coupled to the primary and secondary processing units and contains a control algorithm. The primary and secondary processing units are adapted to run the control algorithm. The functional compare module is coupled to the primary processing unit and the secondary processing unit and compares a primary output of the primary processing unit and a secondary output of the secondary processing units after the control algorithm has been run by the primary and secondary processing units.

As discussed above, neither Fennel nor Heugel disclose each and every element of independent claim 20. Therefore, applicants respectfully assert that the §103(a) rejection is improper and request that it be withdrawn.

Claims 21-22, 24-28, and 32-33 are ultimately dependent upon allowable claim 20. Therefore, for the reasons set forth above and based on their own merits, applicants respectfully assert that claims 21-22, 24-28 and 32-33 are allowable.

Independent 34 claim sets forth a method for detecting a fault in a controller for use in a motor vehicle. The controller includes a primary processing unit, a secondary processing unit coupled to the primary processing unit, and a common memory coupled to the secondary and primary processing units. The method includes the steps of reading a control algorithm stored in the common memory by the primary processing unit, and reading the control algorithm stored in the common memory source by the secondary processing unit, and comparing a primary output of the primary processing unit and a secondary output of the secondary processing unit and responsively detecting a fault.

As discussed above, neither Fennel nor Heugel disclose each and every step of the claimed invention. Thus, applicants respectfully assert that the §103(a) rejection of claim 34 is improper and request that it be withdrawn.

Claims 39, 40, 41, and 45 are ultimately dependent upon allowable claim 34. Thus, for the reasons set forth above, and based on their own merits, applicants respectfully assert that claims 39, 40 and 45 are allowable and request that the §103(a) rejection be withdrawn.

Independent claim 47 sets for a controller for a motor vehicle. The controller includes primary and secondary processing units, a common memory, and a functional compare module. The primary processing unit is coupled to the motor vehicle and performs a first set of functions. The secondary processing unit is coupled to the motor vehicle and to the primary processing unit and performs a set of primary test functions. The common memory is coupled to the primary and secondary processing units and contains a control algorithm. The primary processing unit is adapted to run the control algorithm. The functional compare module is coupled to the primary processing unit and the secondary processing unit and compares a primary output of the primary processing unit after the control algorithm has been run and a test output of the secondary processing unit, and responsively detects a fault in the primary processing unit. The secondary processing unit performs the first set of functions upon detection of a fault in the primary processing unit.

As discussed above, neither Fennel nor Heugel disclose such a structure. Since neither Fennel nor Heugel disclose each and every element of independent claim 47, applicants respectfully assert that the §103(a) rejection of claim 47 is improper and request that it be withdrawn.

Claims 52, 53, and 58 are ultimately dependent upon allowable claim 47. Thus, for the reasons set forth above, and based on their own merits, applicants respectfully assert that claims 52, 53 and 58 are allowable.

Claims 16, 17, 43, and 44 were rejected under 35 USC §103(a) as being unpatentable over Fennel and Heugel, and in further view of Dutton et al ("Dutton"). This rejection is respectfully traversed.

Claims 16 and 17 are ultimately dependent upon allowable claim 11 and claims 43 and 44 are ultimately dependent upon allowable claim 34. Therefore, for the reasons set forth above, and based on their own merits, applicants respectfully assert that claims 16-17 and 43-44 are allowable and request that the §103(a) rejection be withdrawn.

Claim 23 was rejected under 35 USC §103(a) as being unpatentable over Fennel and Heugel in further view of Discenzo. This rejection is respectfully traversed. Claim 23 is ultimately dependent on allowable claim 20. Thus, for the reasons set forth above and based on its own merits, applicants respectfully assert that the claim 23 is allowable.

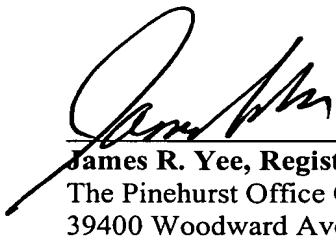
All of the Examiner's objections and rejections having been made moot or successfully traversed, applicants respectfully assert that the present application is now in condition for allowance. An early Notice of Allowance is solicited.

If the Examiner believes that a telephone interview would be helpful, please contact the undersigned at the number below.

Applicant believes that no fees are due, however, if any become required, the Commissioner is hereby authorized to charge any additional fees or credit any overpayments to Deposit Account 08-2789.

Respectfully submitted

HOWARD & HOWARD ATTORNEYS, P.C.



October 18, 2004
Date

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CERTIFICATE OF MAILING

I hereby certify that this Amendment for United States Patent Application Serial Number 10/075,972 filed February 14, 2002 is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on **October 18, 2004**.

Melissa S. Dadisman

JRY/msd